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10/823,030	04/13/2004	Patrick C. Fenton	16437-0209U	3385

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CESARI AND MCKENNA, LLP
88 BLACK FALCON AVENUE
BOSTON, MA 02210

EXAMINER	
NGUYEN, LEON VIET Q	
ART UNIT	PAPER NUMBER
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,030	FENTON, PATRICK C.	
	Examiner	Art Unit	
	LEON-VIET Q. NGUYEN	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31,35,36 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,21,35,36 and 39* is/are rejected.

7)☒ Claim(s) *11-20 and 22-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/23/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/23/09 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 4/23/09 was filed after the mailing date of 4/23/09. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 11/088,357.

Regarding claim 1, "an array of complex accumulation registers that over multiple code chips accumulate measurements that correspond to samples of the received signal, the accumulation registers being associated with a code chip range that spans a portion of a code chip that is less than the entire code chip" corresponds to "an array of complex accumulation registers that over multiple code chips accumulate correlation measurements that correspond to samples of the received signal, the complex accumulators being associated with code chip ranges that span all or a portion of one or more code chips" of claim 1 in copending Application No. 11/088,357; and

"a code phase decoder that controls the respective complex accumulation registers to direct respective measurements to the complex accumulation registers that are associated with the code chip ranges from which the samples are taken, the code phase decoder decoding values that correspond to the estimated phase angles of the sample" corresponds to "a code phase decoder that controls the complex accumulation registers to direct respective correlation measurements to the complex accumulation

registers that are associated with the code chip ranges from which the samples are taken, the code phase decoder decoding values that correspond to estimated code phase times of the samples" of claim 1 in of copending Application No. 11/088,357.

Although copending Application No. 11/088,357 fails to include the limitation "producing a sum that corresponds to the associated code chip ranges", it is well known in the art that accumulators produce a sum.

This is a provisional obviousness-type double patenting rejection.

5. Claims 10 and 21 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14-16 of copending Application No. 11/226,174.

Regarding claims 10 and 21, "a local code generator that produces phase-delayed versions of a code that is included in the received signal" corresponds to "a local code generator that produces a phase-delayed version of a first PRN code that is included in the first channel of the received signal" in claim 14;

"a plurality of multipliers that multiply the respective versions of the code by samples taken of the received signal and produce corresponding measurements" corresponds to "a plurality of multipliers that multiply the respective versions of the code by samples taken of the first channel of the received signal and produce corresponding measurements" in claim 16;

"a code phase generator that produces chip edge signals and code phase angles that correspond to an estimated code phase" corresponds to "a code phase generator that produces chip edge signals and code phase angles that correspond to an estimated code phase of the first PRN code" in claim 14;

"a carrier phase generator that produces phase angles that correspond to an estimated carrier phase" corresponds to "a carrier phase generator that produces phase angles that correspond to an estimated carrier phase of the first signal channel of the received signal" in claim 14;

"a code tracking delay lock loop that produces code error signals that are used to control the code rate of the code generator" corresponds to "a code tracking delay lock loop that produces code error signals that are used to control the code rate of the code generator" in claim 16;

"a carrier tracking phase lock loop that produces phase error signals that are used to control the phase generator" corresponds to "a carrier tracking phase lock loop that produces phase error signals that are used to control the phase generator" in claim 16;

a pre-correlation filter that includes

"an array of complex accumulation registers that collect measurements that correspond to samples of the received signal, the accumulation registers being associated with code chip ranges that span all or a portion of a code chip" corresponds to "an array of complex accumulation registers that collect measurements that correspond to samples of the first channel of the received signal over multiple code

chips of the first PRN code, the respective accumulation registers being associated with code chip ranges that span all or a portion of a code chip of the first PRN code" in claim 14;

"a code phase decoder that controls the complex accumulation registers to direct the measurements to the respective complex accumulation registers that are associated with the code chip ranges from which the associated samples are taken, the code phase decoder decoding values that correspond to the estimated phase angles of the samples" corresponds to "one or more code phase decoders that control the complex accumulation registers to direct the measurements to the respective complex accumulation registers that are associated with the code chip ranges from which the associated samples are taken, the one or more code phase decoders decoding values that correspond to the estimated phase angles of the samples in the first PRN code" in claim 14;

"a multipath mitigation processor that uses the measurements collected by the complex accumulation registers to produce code multipath error signals and carrier multipath error signals" corresponds to "a multipath mitigation processor that uses the measurements collected by the complex accumulation registers to produce code multipath error signals and carrier multipath error signals; and adders that combine the code multipath error signals" in claim 15; and

"adders that combine the code multipath error signals and carrier multipath error signals with the code error signals and phase errors signals, respectively, to correct for code and carrier tracking errors associated with multipath interference, the adders

producing the signals that are used to control the code generator and the phase generator" corresponds to "adders that combine the code multipath error signals and carrier multipath error signals with the code error signals and phase errors signals, respectively, to correct for code and carrier tracking errors associated with multipath interference, the adders producing the signals that are used to control the code generator and the phase generator" in claim 15.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al (US20020181632) in view of Fenton et al (US6243409), hereby referred to as Fenton409, and further in view of Fenton et al (US5390207), hereby referred to as Fenton207.

Re claim 1, Kang teaches a pre-correlation filter for a receiver that receives spread-spectrum signals (fig. 4), the filter including:

an array of complex accumulation registers (m/2 complex adders in fig. 7) that over multiple code chips accumulate measurements (¶0029, each hypothesis includes a

96-chip sequence which is interpreted to be a code chip) that correspond to samples of the received signal (¶0024, samples received over data signal s20), and producing a sum (¶0030, the correlation result from integrator 140) that corresponds to an associated code chip range that spans a portion of a code chip that is less than the entire code chip (fig. 8, the correlation results for a 32 chip range. The 96-chip burst is interpreted to be the entire code chip); and

a code phase decoder (130 in fig. 4) that controls the respective complex accumulation registers to direct respective measurements to the complex accumulation registers that are associated with the code chip ranges from which the samples are taken (¶0030, decoder sends a product vector to the adders within integrator 140 depicted in fig. 7),

Kang fails to teach wherein each accumulation register is associated with a code chip range that span only a portion of a code chip that is less than the entire code chip and

the code phase decoder decoding values that correspond to the estimated code phase angles of the sample.

Fenton409 teaches an accumulation register (correlators 22a-22d in fig. 2, col. 5 lines 35-38, the correlators perform accumulation) wherein each accumulator register is associated with a code chip range that span only a portion of a code chip that is less than the entire code chip (col. 2 line 66 – col. 3 line 6, it would be obvious to use the

blanked-PRN code from block 30 in fig. 1 in correlators 22a-22d in fig. 2 with each PRN code comprising a small fraction of a code chip).

Therefore taking the combined teachings of Kang and Fenton409 as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of Fenton409 into the apparatus of Kang. The motivation to combine Fenton409 and Kang would be to avoid the consequences associated with using too narrow a delay spacing for narrow correlators (col. 3 lines 12-15 of Fenton409).

Fenton207 teaches a code phase decoder (synchronizer 220 in fig. 3) decoding values that correspond to the estimated code phase angles of a sample (col. 10 lines 22-26 and lines 34-36) which are then sent to an accumulator (col. 10 lines 34-37).

Therefore taking the combined teachings of Kang and Fenton207 as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of Fenton207 into the apparatus of Kang. The motivation to combine Fenton207 and Kang would be to achieve noise reduction (col. 3 lines 53-55 of Fenton207).

Re claim 8, the modified invention of Kang teaches wherein the respective complex accumulation registers include inphase registers (register 244i in fig. 6 of Fenton207) that collect measurements that correspond to inphase samples and

quadrature phase registers (register 244q in fig. 6 of Fenton207) that collect measurements that correspond to quadrature samples.

Re claim 9, the modified invention of Kang teaches wherein the array of complex accumulation values (col. 10 lines 56-57 of Fenton207, the I_D and Q_D data) are compared with a predetermined reference shape to detect the presence or absence of interfering signals (col. 10 lines 56-57 of Fenton207, the low frequency filtering function is interpreted to be the reference shape).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al (US20020181632), Fenton et al (US6243409), hereby referred to as Fenton409, and Fenton et al (US5390207), hereby referred to as Fenton207, in view of Stansell, Jr. (US5963582).

Re claim 2, the modified invention of Kang fails to teach a pre-correlation filter wherein the code chip ranges covering a rising edge of the code chip are smaller than the code chip ranges covering other sections of the code chip. However Stansell, Jr. teaches the leading edge of a code chip being smaller than other sections of the code chip (fig. 36G, col. 43 lines 15-17).

Therefore taking the modified teachings of Kang, Fenton409 and Fenton207 with Stansell, Jr. as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the smaller leading edge of a code chip

of Stansell, Jr. into the pre-correlation filter of Kang, Fenton409, and Fenton207. The motivation to combine Stansell, Jr., Kang, Fenton409, and Fenton207 would be to simplify the logic (col. 43 lines 18-19 of Stansell, Jr).

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al (US20020181632), Fenton et al (US6243409), hereby referred to as Fenton409, and Fenton et al (US5390207), hereby referred to as Fenton207, in view of Zhengdi (US6751247).

Re claim 3, the modified invention of Kang fails to teach a pre-correlation filter wherein the code chip ranges are adjustable. However Zhengdi teaches changing a code chip frequency, interpreted to be the code chip range, according to the duration in time of the spreading code and according to the chip length (col. 4 lines 29-33).

Therefore taking the modified teachings of Kang, Fenton409 and Fenton207 with Zhengdi as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the adjustable code chip frequency of Zhengdi into the pre-correlation filter of Kang, Fenton409 and Fenton207. The motivation to combine Zhengdi, Kang, Fenton409 and Fenton207 would be to reduce correlation between the spreading codes (col. 4 lines 33-34 of Zhengdi) and detect the signal better (col. 4 line 41 of Zhengdi).

10. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al (US20020181632), Fenton et al (US6243409), hereby referred to as

Fenton409, and Fenton et al (US5390207), hereby referred to as Fenton207, in view of Harms et al (US6493376).

Re claim 4, the modified invention of Kang fails to teach a pre-correlation filter wherein the sizes, numbers and starting points of the code chip ranges are selectively varied. However, in ¶0049 of applicant's specification, varying of the length, number, and/or starting position of the ranges is achieved by changing the code offset values associated with the accumulators.

Harms teaches an accumulator which generates the correlation of the data at each possible local PN code offset time (col. 24 lines 2-5). Although not explicitly stated, one of ordinary skill in the art would have found it obvious and necessary to change the code offset values corresponding to the code offset times.

Therefore taking the modified teachings of Kang, Fenton409 and Fenton207 with Harms as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the changing of code offset values of Harms into the pre-correlation filter of Kang, Fenton409 and Fenton207. The motivation to combine Harms, Kang, Fenton409 and Fenton207 would be to differentially detect phase shifts between consecutive accumulated signals (col. 6 lines 8-12 of Harms).

Re claim 5, the modified invention of Kang teaches a pre-correlation filter wherein the code chip ranges that include an estimated location of the chip edges in a direct path signal are narrowed (col. 3 lines 41-43 of Fenton207).

Re claim 6, the claimed limitations recited have been analyzed and rejected with respect to claim 4.

Re claim 7, the modified invention of Kang teaches a pre-correlation filter wherein the number of code chip ranges is reduced after an estimate of the location of chip edges in a direct path signal is calculated (¶0044 of Kang).

11. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Underbrink et al (US20050025222) in view of Fenton et al (US6243409) and further in view of Harms et al (US6493376).

Re claim 35, Underbrink teaches a method of producing measurement pulse shapes associated with code chips of a PRN code in a received signal, the method including the steps of:

over multiple PRN code chips (¶0013, "one of the PN code chips" it is interpreted to mean that there is more than one code chip) taking measurements that correspond to samples of the received signal (¶0013, the selected portion of the signal sample is interpreted to be a measurement corresponding to that sample); and

selectively combining the measurements into ranges that span a code chip (¶0013, the adder adding the first and second product which corresponds to the measurements from the first and second signal samples), the ranges being based on estimated code phase angles of the samples (¶0014, Underbrink teaches that each pair of signal samples has an in-phase and quadrature-phase portion, which is well known to

have a phase angle. Therefore it is interpreted that the range is based on the phase angles. Furthermore it is well known in the art that in spread spectrum communications, distinct codes are used to differentiate phase angles of each portion of a signal).

Underbrink fails to teach wherein each of the respective ranges span only a portion of a code chip and determining an estimated location of the chip edges in a direct path signal.

However Fenton teaches utilizing a code chip range of a PRN code chip that spans only a portion of the code chip (col. 2 line 66 – col. 3 line 6, it would be obvious to use the blanked-PRN code from block 30 in fig. 1 in correlators 22a-22d in fig. 2 with each PRN code comprising a small fraction of a code chip) and determining an estimated location of the chip edges in a direct path signal (col. 7 lines 16-19).

Therefore taking the combined teachings of Underbrink and Fenton as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of Fenton into the method of Underbrink. The motivation to combine Fenton and Underbrink would be to avoid the consequences associated with using too narrow a delay spacing for narrow correlators (col. 3 lines 12-15 of Fenton).

Underbrink also fails to teach changing the starting points of one or more code chip ranges to selectively position the code chip ranges relative to the estimated location of chip edges in a direct path signal. However, in ¶0049 of applicant's

specification, varying of the length, number, and/or starting position of the ranges is achieved by changing the code offset values associated with the accumulators.

Harms teaches an accumulator which generates the correlation of the data at each possible local PN code offset time (col. 24 lines 2-5). Although not explicitly stated, one of ordinary skill in the art would have found it obvious and necessary to change the code offset values corresponding to the code offset times.

Therefore taking the modified teachings of Underbrink with Harms as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the changing of code offset values of Harms into the method of Underbrink. The motivation to combine Harms and Underbrink would be to differentially detect phase shifts between consecutive accumulated signals (col. 6 lines 8-12 of Harms).

12. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Underbrink et al (US20050025222), Fenton et al (US6243409) and Harms et al (US6493376) in view of Zhengdi (US6751247).

Re claim 36, the modified invention of Underbrink fails to teach a method wherein the code chip ranges are reduced. However Zhengdi teaches changing a code chip frequency, interpreted to be the code chip range, according to the duration in time of the spreading code and according to the chip length (col. 4 lines 29-33). One of ordinary skill in the art in the art would have found it obvious to reduce the code chip frequency which would effectively reduce the number of ranges.

Therefore taking the modified teachings of Underbrink, Fenton, and Harms with Zhengdi as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of Zhengdi into the method of Underbrink, Fenton, and Harms. The motivation to combine Zhengdi, Underbrink, Fenton, and Harms would be to reduce correlation between the spreading codes (col. 4 lines 33-34 of Zhengdi) and detect the signal better (col. 4 line 41 of Zhengdi).

13. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Underbrink et al (US20050025222) in view of Fenton et al (US6243409) and further in view of Garin et al (US20060095206).

Re claim 38, Underbrink teaches a method of producing measurement pulse shapes associated with code chips of a PRN code in a received signal, the method including the steps of:

over multiple PRN code chips (¶0013, "one of the PN code chips" it is interpreted to mean that there is more than one code chip) taking measurements that correspond to samples of the received signal (¶0013, the selected portion of the signal sample is interpreted to be a measurement corresponding to that sample); and

selectively combining the measurements into ranges that span a code chip (¶0013, the adder adding the first and second product which corresponds to the measurements from the first and second signal samples), the ranges being based on estimated code phase angles of the samples (¶0014, Underbrink teaches that each pair of signal samples has an in-phase and quadrature-phase portion, which is well known to

have a phase angle. Therefore it is interpreted that the range is based on the phase angles. Furthermore it is well known in the art that in spread spectrum communications, distinct codes are used to differentiate phase angles of each portion of a signal).

Underbrink fails to teach a method wherein each of the respective ranges span only a portion of a code chip and combining the measurements to produce one or more early correlation values and one or more late correlation values for use in correlating a local PRN code to the received PRN code and a local carrier to a received carrier. However Fenton teaches wherein each of the respective ranges span only a portion of a code chip (col. 2 line 66 – col. 3 line 6, it would be obvious to use the blanked-PRN code from block 30 in fig. 1 in correlators 22a-22d in fig. 2 with each PRN code comprising a small fraction of a code chip) and combining the measurements to produce one or more early correlation values and one or more late correlation values (col. 1 lines 49-55) for use in correlating a local PRN code to the received PRN code (col. 1 lines 55-59) and a local carrier to a received carrier (col. 1 lines 62-65).

Therefore taking the combined teachings of Underbrink and Fenton as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of Fenton into the method of Underbrink. The motivation to combine Fenton and Underbrink would be to avoid the consequences associated with using too narrow a delay spacing for narrow correlators (col. 3 lines 12-15 of Fenton).

Underbrink also fails to teach producing code offset and carrier phase values for use in controlling a local code phase generator and a local carrier phase generator respectively. However Garin teaches producing code offset (processor 502 in fig. 5, the offset value from 1102 in fig. 11, ¶0049) and carrier phase values (the output from 212 in fig. 6, ¶0051) for use in controlling a local code phase generator and a local carrier phase generator (¶0049, ¶0054).

Therefore taking the combined teachings of Underbrink and Garin as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of Garin into the method of Underbrink. The motivation to combine Garin and Underbrink would be to correct the effects of Doppler shift (¶0050 of Garin).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON-VIET Q. NGUYEN whose telephone number is (571)270-1185. The examiner can normally be reached on Monday-Friday, alternate Friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Q Nguyen/
Examiner, Art Unit 2611

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611